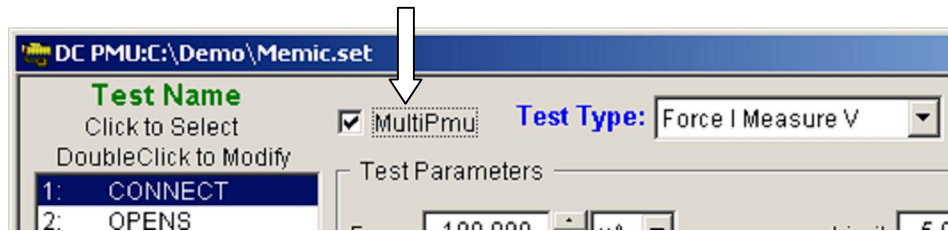


Q: Can DUT Continuity be tested faster?

Continuity Test with Functional Vectors for Mass Production

DUT Continuity can be tested one pin at a time in ETS2K using the DC PMU. Unfortunately, this is a time-consuming and therefore costly approach for Production Test. Since your system includes a DC PMU on every pin card (one for every 32 pins installed), the total test time can be greatly reduced by making the measurements in parallel. For high pincount devices or for MultiSite applications, this will greatly reduce test time. To enable this feature, simply click the Multi PMU checkbox in the DC PMU window:



This setting is saved in the SET file. Be sure to check this box for every DC PMU test you have defined. And if you are using AutoTest, be sure to enable the Special Script "AutoTestUsePmuPer32". Unfortunately, this type of test may not detect pin-to-pin shorts. But there is a technique, able to combine both test speed and ability to detect pin-to-pin shorts at the same time.

The continuity test can be defined as a functional test consisting of only a few vectors, and will employ a unique SET file that is used *only* for continuity checking. For our current forcing, the programmable dynamic loads will be used. This is a per-pin resource where the commutation voltage, source current, and sink current can be programmed in software. For this method of continuity test, the programmable loads will be set to 0mA source current (I_{OL}) and 100uA sink current (I_{OH})¹. Since the voltage drop across a normally operating diode is no more than 800mV, the commutation voltage will be set to -1.2V to provide enough voltage separation for our Pass/Fail detection. The tester comparators will be used to compare the voltage drop against our test limits. Two tests need to be performed; one for shorts detection, and a second for opens detection.

Pin-to-Pin Shorts Setup

The pin-to-pin shorts test can be performed at the same time as the shorts test. The test is accomplished by testing every other pin for continuity on one pass, while other pins are grounded. Then the remaining pins can be tested with a second pass while the previously tested pins are grounded. When we say "grounded" for this application, we mean the pin driver is set to 0V by driving a logic LO in the vectors. Since the HiLevel driver output impedance is 50 Ohms and the typical continuity force current is 100uA, the expected voltage drop is 5mV. The typical voltage drop on protective diodes is at least 300mV, so there is enough separation between those two conditions for our test.

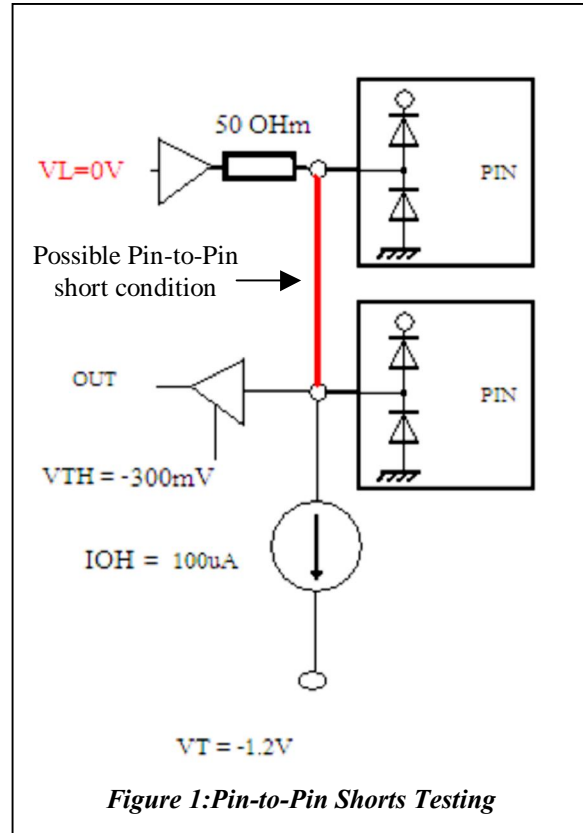
Figure 1 illustrates our Pin-to-Pin shorts test method.

¹ These current settings can be any value given by your device specification.

Switching between pins for the test can be achieved by defining each device pin in our Continuity SET file as an I/O pin. For Continuity test purposes, all of our device pins may be in one group, provided that every pin of the device has the same electrical characteristics.

The functional test pattern for our shorts test will consist of five vectors. First, every even pin will be grounded (that is, the tester will drive logic zero) while testing the odd pins for Output LO (below 300mV). Then the odd pins will be grounded while even pins are tested.

When we say odd or even pins, it is important to note that this is a generic way of identifying adjacent pins of the device and not simply applying odd and even tester channel numbers. For example, on a DIP package it is easy to determine odd and even pin numbers, but on a large pincount BGA package more study is required. It is unlikely that a device pin on one side of a package could be shorted to a device pin on the other side, so where the pins connect to the die is perhaps the most important approach. Still, the method defined here is generally very effective for a fast continuity test solution, even though we will illustrate using tester channels in sequence for clarity.



Shorts Detection

In a single run of one functional pattern, a pin short can be detected whether it is shorted to power or ground, or shorted to another pin. All of our pins are expected to show voltage drop of more than 300mV, so we will set our compare threshold voltage to 300mV below zero. Thus all the pins are expected to be in a logic low state (L) with a voltage lower than 60.300V in order to pass. See figure 2.

