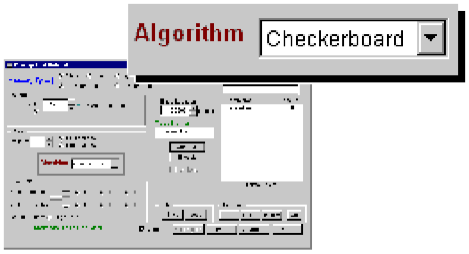
HILEVEL Technology, Inc.

Q'n Apps #P36

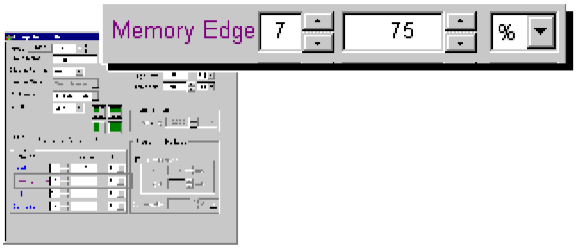
Q: What is the functional description of HiLevel's Memory Test feature?

Memory Test Functional Description

Stimulus Data has special meaning when the ETS is in Memory Test mode. Each byte of stimulus data (for memory address/data only) controls special functions within the Memory Test circuitry of the Pin Electronics. The specific functions are determined by the selected ***Algorithm.***



Memory Test



Pin Setup

Stimulus Values Pertaining to Memory Test

When referencing the table below, refer also to the **Memory Test Functional Diagram.** The following information applies to each *byte* of stimulus data for both address and data. Note that stimulus bit 7 functions as a strobe to the memory test circuit and is indicated as ***Memory Edge*** in the Pin Setup Window. ***Edge*** refers to the 'active' edge of the strobe.

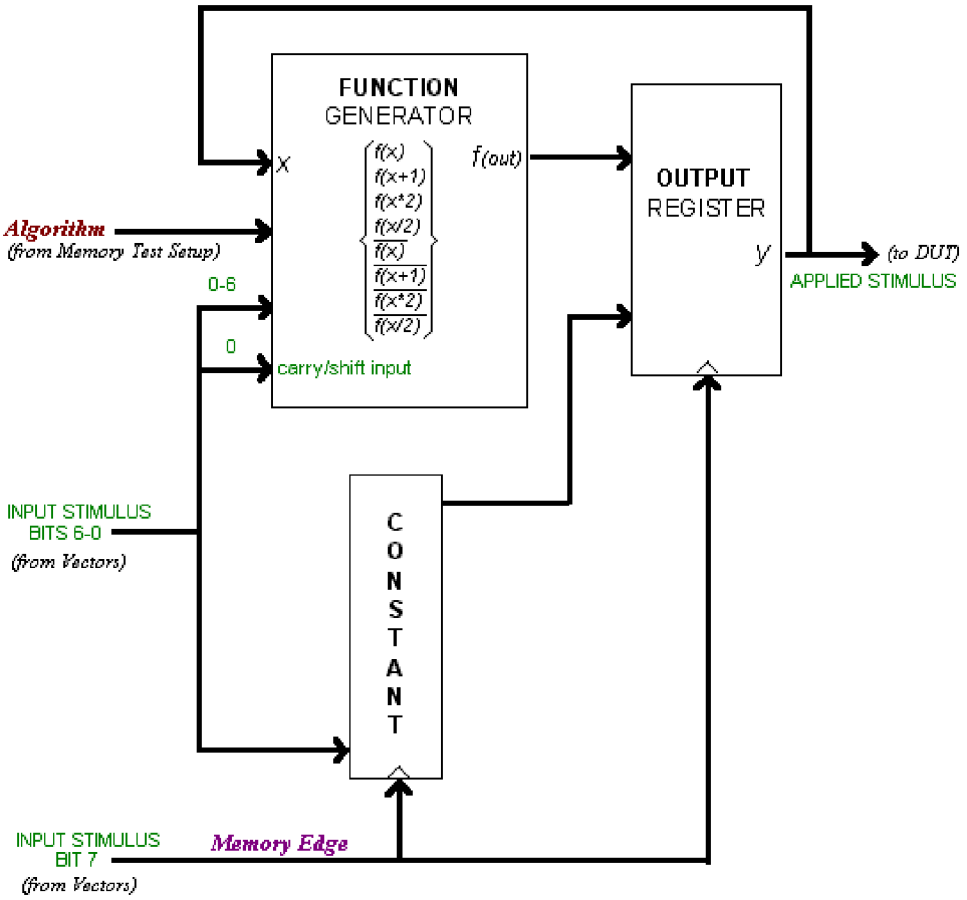
Stimulus	**Function**	**Comments**
0x00-0x01	**NOOP**	
0x90	*y* = **CONSTANT** used	Most commonly used to load/reload initial value by the specified ***Algorithm***
0xA0	*y = f(x)* *y = f(x*2)* *y = f(x/2)*	Output previous result (effectively a NOOP) Shift left one bit position, insert '0' Shift right one bit position, insert '0'
0xA1	*y = f(x+1)* *y = f(x*2)* *y = f(x/2)*	Increment Shift left one bit position, insert '1' Shift right one bit position, insert '1'
0xB0	$y = \overline{f(x)}$	Complement.
0xB1	$y = \overline{f(x) + 1}$	
0xC0-0xCF	Load **CONSTANT**	LS 4 bits are loaded into LS byte of 32-bit **CONSTANT** (bits 0-27 of **CONSTANT** are left-justified).

NOTE: The specific **FUNCTION** (increment, shift) is determined by the selected ***Algorithm.*** The input vectors have direct control over carry/serial input, complement, loading of **CONSTANT** register only.

Bit 7 of each stimulus byte is an RZ stimulus bit. This stimulus bit clocks the **FUNCTION** results into the **OUTPUT** register of the memory test circuit and loads/shifts data into **CONSTANT**, four bits at a time. The trailing (clocking) edge of this stimulus bit is defined by ***Memory Edge*** in **Pin Setup.**

Under normal operation, vector data is applied to the DUT exactly as defined in Pin Setup. However, when Memory Test is selected, vector data controls special functions used in the generation of specific patterns which are determined by selected algorithms. Therefore, the expected response data reflects the response expected as a result of the applied stimulus from the Memory Test circuit and not the Vector Stimulus. For example, if a Checkerboard pattern is chosen under **Algorithms** in Memory Test Setup, the expected response will be either 0x**55** or 0x**AA**, while the vector stimulus will appear as previously defined under **Stimulus Values Pertaining to Memory Test**. In order to ease confusion and facilitate debug/verification, a special 'Pin Direction' is automatically selected in Pin Setup**.** *'Split Memadr' and 'Split Memdata'* allow the user to view (in the Analysis screen) Stimulus Data both as it is input to the Pin Electronics (to Memory Test), and as it is input to the DUT (from Memory Test) within the same test cycle.

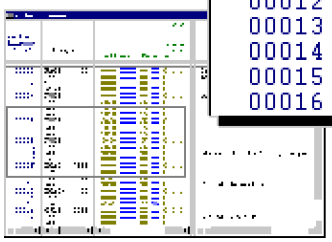
The diagram below applies both to memory address and memory data. It is repeated for each byte of address or data. Also, see **Example 1** on the next page.



Memory Test Functional Diagram

Memory Test Vectors

Vector Address (Hex)	Program	Address	Data	Write	OE	CE
00005	NOOP	C0C0 XXXX	C5 XX	0	1	1
00006	NOOP	C0C0 XXXX	C5 XX	0	1	1
00007	NOOP	C0C0 XXXX	C5 XX	0	1	1
00008	NOOP	C0C0 XXXX	C5 XX	0	1	1
00009	NOOP	C0C0 XXXX	C5 XX	0	1	1
0000A	NOOP	C0C0 XXXX	C5 XX	0	1	1
0000B	NOOP	C0C0 XXXX	C5 XX	0	1	1
0000C	NOOP	C0C0 XXXX	C5 XX	0	1	1
0000D	NOOP	9090 XXXX	90 XX	0	1	1
0000E	LOADX 00	0000 XXXX	00 XX	0	1	1
0000F	LOAD 7FFF	0000 XXXX	00 XX	0	1	1
00010	DEC	0000 XXXX	00 XX	0	1	1
00011	LOOP 0011	A1A1 XXXX	B0 XX	1	1	0
00012	NOOP	9090 XXXX	90 XX	0	1	1
00013	LOADX 00	0000 XXXX	00 XX	0	1	1
00014	LOAD 3FFF	0000 XXXX	00 XX	0	1	1
00015	DEC	A1A1 XXXX	ZZ 55	0	0	0
00016	CJMP 0015	A1A1 XXXX	ZZ AA	0	0	0



Vectors

00005-0000C Loads '**00000000**' into 32-bit **CONSTANT** for each byte of address stimulus.
Loads '**55555555**' into 32-bit **CONSTANT** for data stimulus.

0000D Loads **OUTPUT** Registers with **CONSTANTS** for address and data stimuli. (i.e. address='0000', data='55' - See NOTE)

0000E-00010 Performs no operation relative to memory stimulus. These vectors set up the loop count in preparation for generating memory write stimulus.

00011 This vector increments the address and complements the data stimulus for each test cycle (determined by **Memory Edge** timing). The test loops on this vector (decrementing the loop count each cycle), until the count reaches zero.

00012 Loads **OUTPUT** Registers with **CONSTANTS** (i.e. address='0000', data='55')

00013-00014 No operation for memory stimulus. Sets up loop count in preparation for generating memory read stimulus. Note that the loop count reflects the fact that there are 2 memory read cycles for each decrement of the count.

00015 Compares memory data (from DUT) with expected data '**55**' and increments the address stimulus. The loop count is decremented.

00016 Compares memory data (from DUT) with expected data '**AA**' and increments the address stimulus. If the loop count has not decremented to zero, vector **00015** is repeated.

NOTE: Although only 15 bits of address and 8 bits of data are significant, all functions are performed with 32-bit operands.

Example 1

Also See: **Q'nApp #P1**: PinList
Q'nApp #P4: Using Memory Test