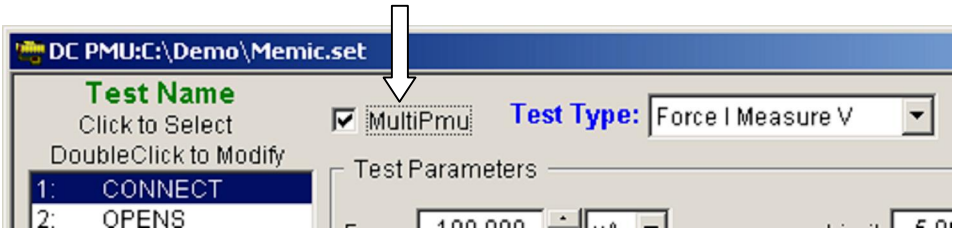
HILEVEL Technology, Inc.

Q'n Apps #P51

Q: Can DUT Continuity be tested faster?

Continuity Test with Functional Vectors for Mass Production

DUT Continuity can be tested one pin at a time in Presto using the DC PMU. Unfortunately, this is a time-consuming and therefore costly approach for Production Test. Since your system includes a DC PMU on every pin card (one for every 32 pins installed), the total test time can be improved by making the measurements in parallel. For high pincount devices or for MultiSite applications, this will greatly reduce test time. To enable this feature, simply click the Multi PMU checkbox in the DC PMU window:



This setting is saved in the SET file. Be sure to check this box for every DC PMU test you have defined. And if you are using AutoTest, be sure to enable the Special Script ñAutoTestUsePmuPer32ò. Unfortunately, this type of test may not detect pin-to-pin shorts. But there is a technique, able to combine both test speed and ability to detect pin-to-pin shorts at the same time.

The continuity test can be defined as a functional test consisting of only a few vectors, and will employ a unique SET file that is used *only* for continuity checking. For our current forcing, the programmable dynamic loads will be used. This is a per-pin resource where the commutation voltage, source current, and sink current can be programmed in software. For this method of continuity test, the programmable loads will be set to 0mA source current (I_{OL}) and 100uA sink current (I_{OH})[1]. Since the voltage drop across a normally operating diode is no more than 800mV, the commutation voltage will be set to -1.2V to provide enough voltage separation for our Pass/Fail detection. The tester comparators will be used to compare the voltage drop against our test limits. Two tests need to be performed; one for shorts detection, and a second for opens detection.

Pin-to-Pin Shorts Setup

The pin-to-pin shorts test can be performed at the same time as the shorts test The test is accomplished by testing every other pin for continuity on one pass, while other pins are grounded. Then the remaining pins can be tested with a second pass while the previously tested pins are grounded. When we say ñgroundedò for this application, we mean the pin driver is set to 0V by driving a logic LO in the vectors. Since the HiLevel driver output impedance is 50 Ohms and the typical continuity force current is 100uA, the expected voltage drop is 5mV. The typical voltage drop on protective diodes is at least 300mV, so there is enough separation between those two conditions for our test.

Figure 1 illustrates our Pin-to-Pin shorts test method.

[1] These current settings can be any value given by your device specification.

Switching between pins for the test can be achieved by defining each device pin in our Continuity SET file as an I/O pin. For Continuity test purposes, all of our device pins may be in one group, provided that every pin of the device has the same electrical characteristics.

The functional test pattern for our shorts test will consist of five vectors. First, every ñevenò pin will be grounded (that is, the tester will drive logic zero) while testing the ñoddò pins for Output LO (below ï 300mV). Then the ñoddò pins will be grounded while ñevenò pins are tested.

When we say ñoddò or ñevenò pins, it is important to note that this is a generic way of identifying adjacent pins of the device and not simply applying odd and even tester channel numbers. For example, on a DIP package it is easy to determine odd and even pin numbers, but on a large pincount BGA package more study is required. It is unlikely that a device pin on one side of a package could be shorted to a device pin on the other side, so where the pins connect to the die is perhaps the most important approach. Still, the method defined here is generally very effective for a fast continuity test solution, even though we will illustrate using tester channels in sequence for clarity.

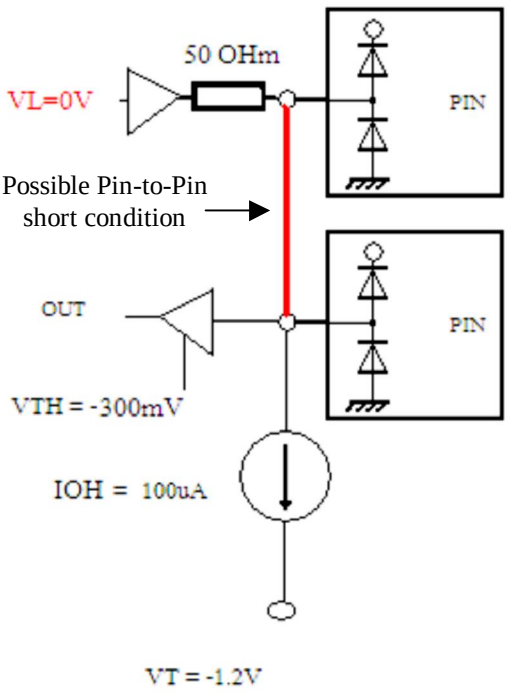
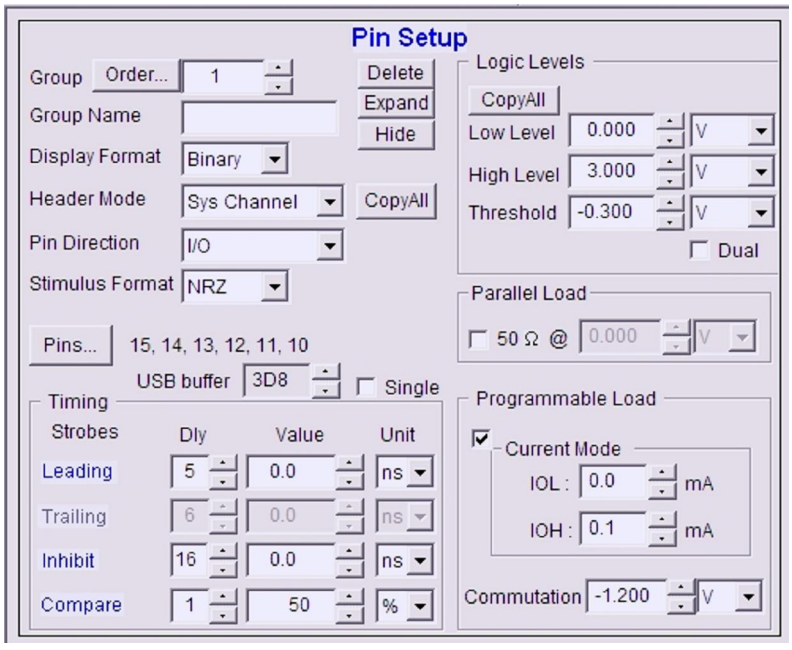


Figure 1:Pin-to-Pin Shorts Testing

Shorts Detection

In a single run of one functional pattern, a pin short can be detected whether it is shorted to power or ground, or shorted to another pin. All of our pins are expected to show voltage drop of more than 300mV, so we will set our compare threshold voltage to 300mV below zero. Thus all the pins are expected to be in a logic low state (L) with a voltage lower than ï 0.300V in order to pass. See figure 2.



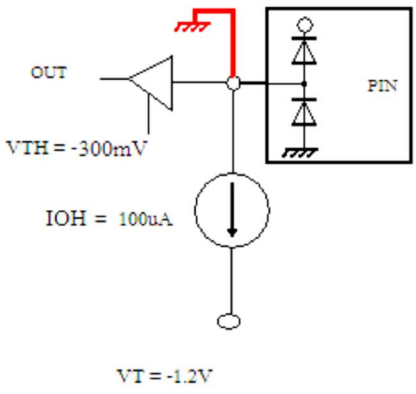
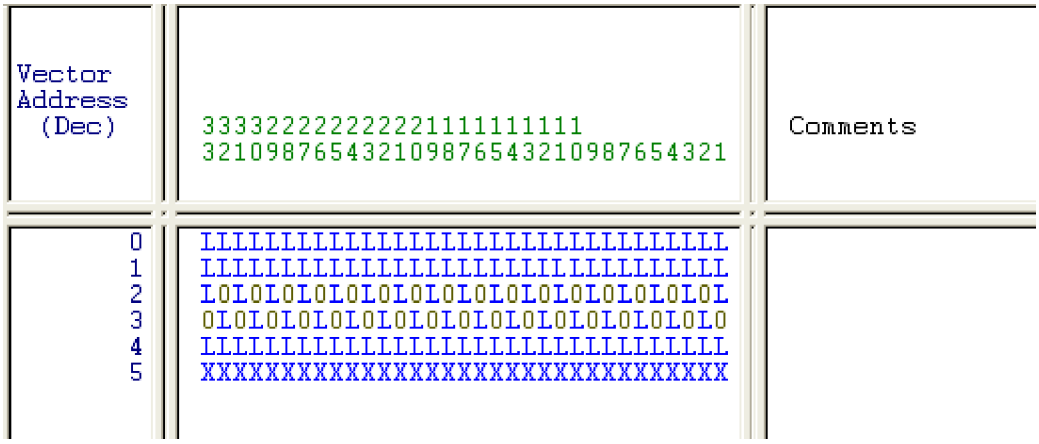


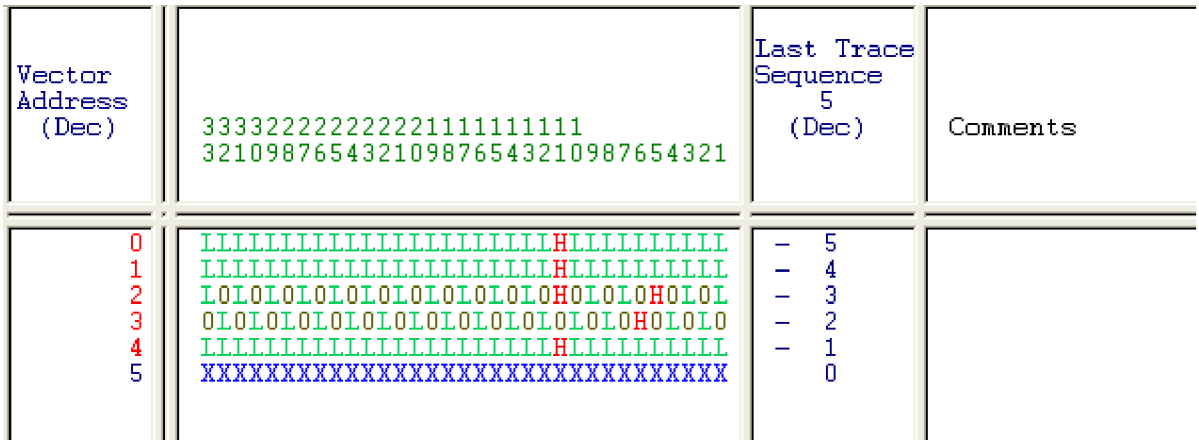
Figure 2: Shorts Test Pin Setup



Vector Address (Dec)	33332222222222111111111 32109876543210987654321	Comments
0	LLLLLLLLLLLLLLLLLLLLLLLLLLLLLLL	
1	LLLLLLLLLLLLLLLLLLLLLLLLLLLLLLL	
2	LOLOLOLOLOLOLOLOLOLOLOLOLOLOLOL	
3	OLOLOLOLOLOLOLOLOLOLOLOLOLOLOLO	
4	LLLLLLLLLLLLLLLLLLLLLLLLLLLLLLL	
5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	

Figure 3: Vectors for Shorts Test

Viewing the vectors in figure 3, we can see that any pin presenting logic High (that is, a voltage higher than ï 300mV) will cause a functional test fail. From an automated Production test standpoint, a failure of this functional test means that at least one pin of the device is shorted; it may be logged as ñFailedò and the tester moves on to the next device. Functional test failure results can be saved for later analysis and failing pins determined as a post-processes effort. Figure 4 shows how a shorts failure will look in analysis.



Vector Address (Dec)	33332222222222111111111 32109876543210987654321	Last Trace Sequence 5 (Dec)	Comments
0	LLLLLLLLLLLLLLLLLLLLLHLLLLLLLLLL	– 5	
1	LLLLLLLLLLLLLLLLLLLLLHLLLLLLLLLL	– 4	
2	LOLOLOLOLOLOLOLOLOLOLOHOLOLOHOLOL	– 3	
3	OLOLOLOLOLOLOLOLOLOLOLOLOLOHOLOLO	– 2	
4	LLLLLLLLLLLLLLLLLLLLLHLLLLLLLLLL	– 1	
5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	0	

Figure 4: Analysis results showing failure of Shorts test

In figure 4, we see that pin 11 is shorted, either to power or to ground. Pins 6 and 5 are shorted together because they only fail vectors 2 and 3, not the entire vector range as in pin 11.

Opens Detection

Testing for opens requires a different SET file and vector file. With the programmable loads set as before, the threshold voltage is now set to 800mV below zero, the maximum acceptable voltage drop across the protective diode (unless your specifications define it differently). See figure 5.

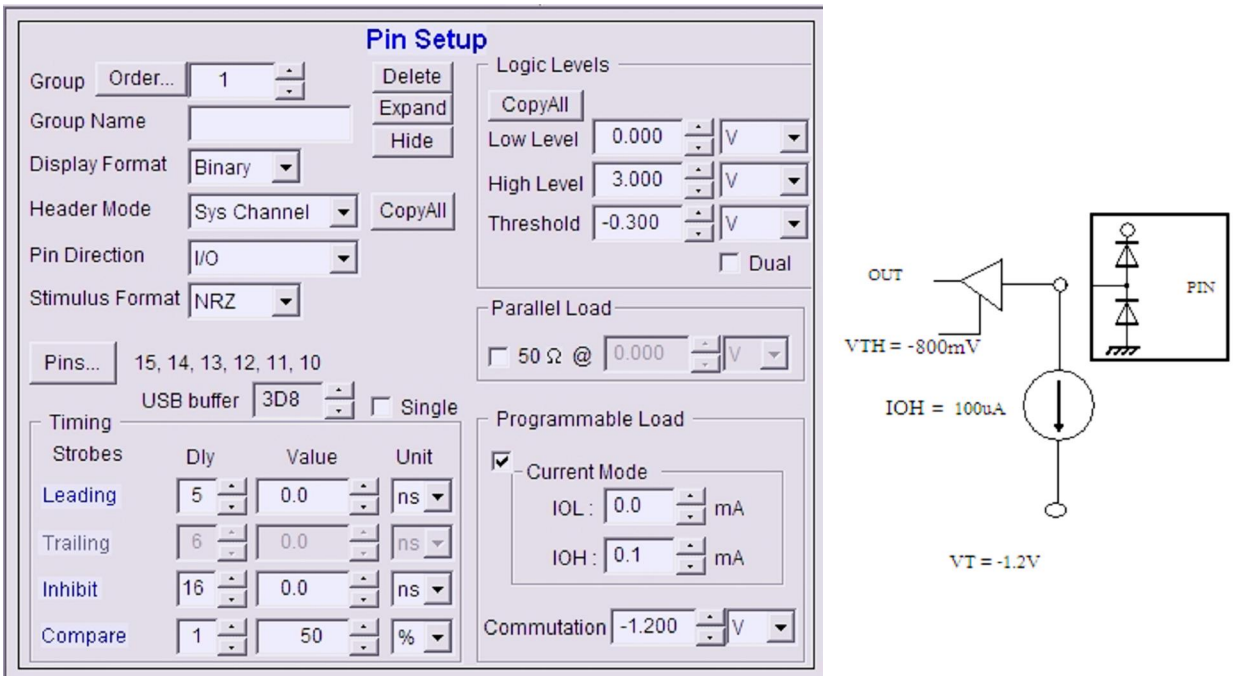
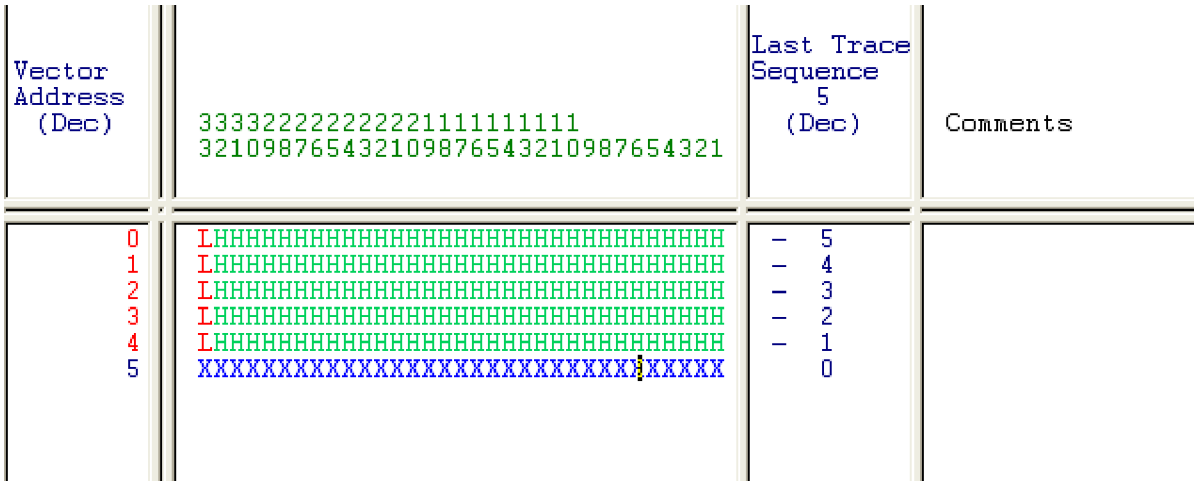


Figure 5: Opens Test Pin Setup

The expected voltage on every pin should be above this threshold limit; therefore all pins should appear as logic High. Any pin with a voltage below -800mV will be considered logic Low and cause functional test fail. Please note that for opens testing, all the pins can be tested in parallel with ñall HIò vectors as shown in figure 6. Again, trace can be saved for later analysis (trace capture results shown in figure 7).

Vector Address (Dec)	33332222222222111111111 32109876543210987654321098765432 1	Comments
0	HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	
1	HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	
2	HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	
3	HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	
4	HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	
5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	

Figure 6: Vectors for Opens test



Vector Address (Dec)	33332222222221111111111 32109876543210987654321098765432 1	Last Trace Sequence 5 (Dec)	Comments
0	LHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	– 5	
1	LHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	– 4	
2	LHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	– 3	
3	LHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	– 2	
4	LHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH	– 1	
5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	0	

Figure 7: Analysis results of Opens test failure

Conclusion

The ability to detect all three types of continuity issues -- opens, shorts, and pin-to-pin shorts -- has been practically proven in the field. Test results conform to the theoretical calculations, and the overall test time for all three continuity tests is equal to the time for a single DC PMU measurement. For mass production, this approach not only contributes to reduced test time, but also improves process quality by detecting pin-to-pin shorts. The ability to save results for later analysis is a valuable tool for process improvement and higher yields, further reducing overall Production cost.

See also:

Q'nApp #P3: Production test
Q'nApp #P12: AutoTest
Q'nApp #P14: Production test
Q'nApp #P35: Programmable loads, DCPMU