HILEVEL Technology, Inc.

Q'n Apps #P9

Q: How can HILevel help me with IDDQ testing?

IDDQ Testing with Presto

Special resources have been incorporated into HiLevel systems for the purpose of IDDQ testing. Often, IDDQ testing requires long cabling to a probe station and a high degree of accuracy of the power source. To support this critical requirement and maintain better than 1% accuracy with 10mV resolution, HiLevel brought the sense lines for all DUT power supplies out to the DUT board connectors.

Among the types of supported DC parametric testing is IDDQ testing. It is similar to IDD testing in as much as the same circuitry is used, but differs in the sense that all output pins are disconnected thus presenting no load to the chip.

Basically, we run to a vector, open all output pins, and measure the Power supply current. To ensure proper power cycling, it is recommended that the controlled Power Ramp feature be used (see QôA App #P5).

For the most effective use of IDDQ testing, we must make the measurements at vectors where the quiescent current is the lowest, for two reasons;

1) deviations in IDD that are caused by defects such as bridges will often only be in range of nanoAmps. In order to make efficient measurements, the defect should be a significant percentage of IDD to merit the status of "failure".

(2) the measurement instruments used in testing typically "scale down" to find the measured value. For this reason, deviations of nanoAmps may be overlooked if IDDQ measurements are done in the milliAmp or microAmp range.

If the specifications of the device under test do not help to indicate the best conditions under which IDDQ should be measured, assistance from the designer or further simulation may be needed. When it is known that IDDQ must be measured when, say, all outputs are high, use the "Search Pattern" function in the "Vectors" drawer to locate the vector or vectors where the most outputs are high. As an alternative, the AutoFind feature found in the DC PMU can be used.

An important tool pertaining to IDDQ is Liquid Crystal ñhot spotò testing. To better facilitate this powerful technique, the HiLevel system has been equipped with a mode by which the test is started; the DUT runs to a vector, and loops on this vector for a specified amount of time until the power is shut off for a pre-specified time period. The whole process is then restarted and continues until a repeat count is reached or the test is terminated using the HiLevel test box. This mode of test is launched from the Power Ramp dialog box; note that the ñstop vectorò must be specified in the RunSetup window before the test itself can commence.

See also:
Q'nApp #P3: Production test
Q'nApp #P5: Power Ramps
Q'nApps #P11 & 12: The HiLevel TestBox
Q'nApp #P20: Power and Ground
Q'nApp #P22: Bypass capacitors
Q'nApp #P50: Run & Sample
Q'nApp #P59: Current Limit