HILEVEL Technology, Inc.

Q'n Apps #S17

Q: What are the Stimulus Formats?

Stimulus Formats

When stimulus data is forced out to your DUT input pins it may need to be applied in a certain way. We already know, for example, that very often the data must be present at input pins before the clock edge occurs, allowing sufficient setup time. Stimulus formats help us to shape the stimulus data to conform it to follow the needs of your chip. You can select the stimulus for your inputs only in the Pin Setup window. Here's a description of the different types of stimulus formats:

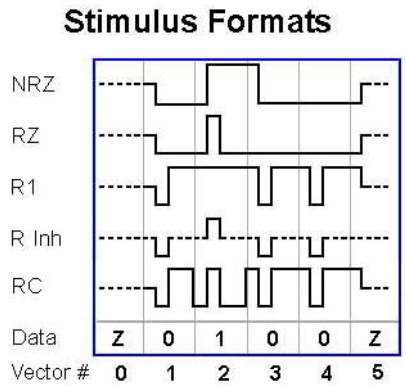
NRZ stands for "Non Return to Zero".
With this format, you can place the delay time for the start of the assertion anywhere in the cycle. Vector data is forced for each vector at a point in time specified by this delay value. It remains asserted for a period equal to one entire test rate clock period. If you specify Leading edge delay to be 10ns, then the stimulus seen at each vector will be "forced" after a 10ns delay from the start of each vector and will continue for 10ns into the next vector. This mode is often used for address pins and non-I/O data pins. Testing your part with all pins defined as NRZ is known as "settled-state" testing, because data is held present on the pins for a much longer period than sometimes necessary to allow everything to "settle" before changing data.

RZ means "Return to Zero".
If a "1" appears in the vector, it is asserted after the leading edge delay time and then the tester driver returns back to zero after the trailing edge time. The duration of the force is:

TT - TL

meaning "trailing time minus leading time". If a zero appears then the output is unchanged for that vector. This format is commonly used for clocks, enables, strobes, and anywhere that control over both edges of stimulus is needed (dynamic data).

R1 means "Return to One".
This dynamic mode of operation performs in much the same way as Return to Zero, except that the active data state is reversed. If a Master Reset pin is active low you can use R1 to hold the pin in the logic high state (i.e., "ones" in the vector data) until a reset is desired, and then apply a logic low (zero in the vector data) for a given period. See the example to compare differences between formats.



R Inh is "Return to Inhibit".
As you can see in the drawing, this mode is a bit similar to R1 or RZ, except that the "Return to" point allows both R1 and RZ to affect change. You must set valid values for Leading and Trailing edges to control duration of the "pulse".

RC Return to Compliment. More accurately, Surround by Compliment. We have retained "RC" as the name because it complies well with the understanding of this format.

Special Note on SCIO
When you select Split Cycle I/O as your data direction and use NRZ as the Stimulus format, your expected data should always be the same as your stimulus data, or else masked when the tester is driving. When your data is in the "Output" mode the tester is not driving, and can capture the output of your DUT. But when the tester is driving, it is unlikely that your DUTs outputs will overcome the tester drivers thereby making a compare only of the drivers state. When using any of the "Dynamic" formats, place your compare strobe away from the "pulse" created by your stimulus data. View your vectors in the Graph window to check your timing.

Also See:
Q'nApp #S1: The PinList function
Q'nApp #S23: Inhibit Delay
Q'nApp #S24: Data vs. Clock
Q'nApp #S25: Drivers & Receivers
Q'nApp #S42: SCIO