HILEVEL Technology, Inc.

Q'n Apps #S24

Q: How does HiLevel define "data" and "clock" rate?

"If you wish to converse with me, define your terms." - Voltaire

For some tester manufacturers, the question of the "true" definition of data rates (or clock rates) has been an issue of "specmanship" more often than it has been of service to those seeking the "truth". Since these variations can be frustrating, we at HiLevel would like to offer *our* definition of data and clock rates and try to help you understand how other views can vary.

What Happens in the tester?

One of the most important points we wish to make clear is that the ETS800 series basic program cycle is 10ns (i.e., 100MHz). This means that data is retrieved from RAM, formatted, processed and driven (as well as received in the case of DUT outputs) all within a *single program cycle,* including loops, branches and other programmed instructions. Not all testers do this; some employ muxing tricks, with the resulting idiosyncrasies. We put a great deal of effort into developing a custom chip specifically for the purpose of performing these operations in a single cycle.

Obviously a higher clock rate compels the need for better resolution. Pin-to-pin skew is equally important for insuring accuracy at higher speeds. At 500MHz, how meaningful is a 2ns cycle time if the edge placement resolution is no better than 100ps? The HiLevel ETS800 delay resolution is 50ps, allowing for excellent resolution in such situations. And where skew relationships are extremely critical, we provide the tools for manual deskew between pins in critical data paths.

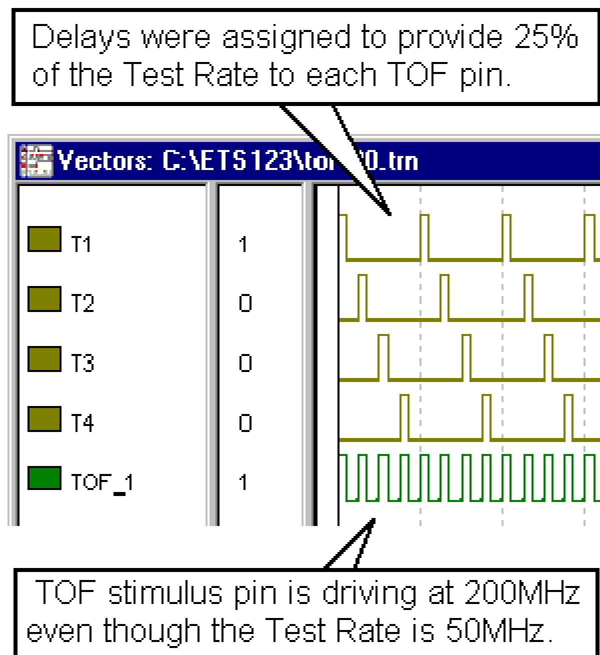
Let us now look at some specifics regarding HiLevel Test Rate, and some discussion about other perceptions of test rates and clock rates.

Bidirectional Data

HiLevel's classification of the basic data rate is somewhat simplistic; the "Test Rate" as defined in the Run Setup window reflects the bidirectional data rate. You can provide stimulus to the device at 2X the data rate (using Timing on the Fly), but the *acquisition* of DUT output data is done at 1X -- in other words, at the defined Test Rate. However, since each channel has dual comparators, you can perform two compares in each cycle and thereby realize up to 200MHz performance (NRZ only).

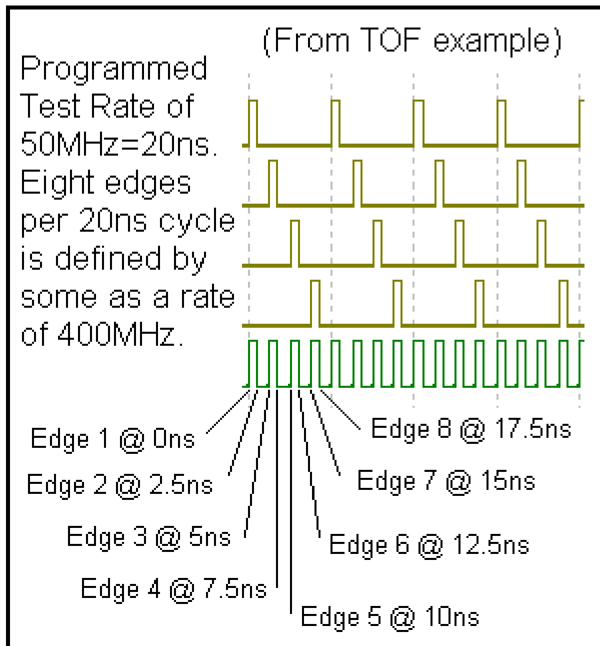
Stimulus Data

To achieve 2X, 3X or 4X stimulus data rate, the Timing On-the-Fly feature is employed (TOF). This feature is covered in the ETS manual and the online Help file that comes with your Symphony software. Some additional system resources are consumed in this mode, but data rates of up to 200MHz are possible with TOF. See the example of how a 200MHz clock is created.



Other Views

Some users and tester manufactures define an edge transition as being the delimiter in determining actual test rate. In other words, if RZ or R1 data format is selected then *two* edge transitions are encountered during each test cycle and the perceived test rate is *double* that of the defined test rate. If this philosophy is employed, the ETS780 (a 50MHz test system) is capable of delivering a **400MHz** stimulus test rate, referring to the example below. However, HiLevel prefers to retain the indisputable premise that the actual "Test Rate" is as defined in the Run Setup window. You may draw your own conclusions regarding views other than the conventional.



An Alternate View of Test Rate Definition

Keep watching for the release of new HiLevel products; sign up on our email list to receive notices automatically! Just go to the signup page at http://www.hilevel.com/emailist.html. You can learn more about HiLevel products on our homepage, including new application notes and announcements of upcoming events.

Also see:

User Manual Section 20: Timing On-the-Fly