HILEVEL Technology, Inc.

Q'nApps #S26

Q: What must be done to prepare for a functional test?

Functional Test On HiLevel Systems

Preparing for functional test is probably easier on the HiLevel systems than any other high performance tester available. That's not our own claim; our customers have stated this time and again. By following the checklist below, you can be sure not to miss any of the important steps in preparation.

Functional test only tests the logic of the device to the thoroughness of your vectors. If you are translating simulation vectors, you should have good fault coverage. If generating vectors by hand it is important that you have a complete truth table or a very intimate knowledge of the device under test.

Use the help windows (accessed by key F1 from any given Symphony window) to help guide you through the set up.

Related info

Q'nApp #E1: Pin List
Q'nApp #S2: Vector Translation
Q'nApp #S13: AutoLearn
Q'nApp #S17: Stimulus Formats
Q'nApp #S19: The Red Question Mark
Q'nApp #S20: Power and Ground
Q'nApp #S22: Bypass Capacitors
Q'nApp #S23: Inhibit Delay
Q'nApp #S24: Clock and Data rates
Q'nApp #S30: Swap Pins
Q'nApp #S34: DUT Boards
Q'nApp #S35: Prog. Loads, DCPMU
Q'nApp #S44: Vector Files W/O Path
Q'nApp #S47: The More Button

Functional Test Checklist

- **Prepare DUT board**
- **Create ASCII pinlist**
- **Invoke Symphony and Initialize**
- **Translate or create functional test vectors**
- **Assign pins and groups (or import pinlist)**
- **Define stimulus format, timing, logic levels**
- **Download test vectors (“L” button)**
- **Define DUT power**
- **Define Test Rate, Last & Stop Vector**
- **Run DUT continuity**
- **Click RUN button and Analyze results**
- **Save SET file one more time**

Be sure to save your SET file as you reach new milestones!